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Result # 1 Relevance: ○○○○○

Method for indirect branch prediction using a memory hierarchy

21-Sep-2005 IPCOM000128941D English (United States)

Disclosed is a method for indirect branch prediction using a memory hierarchy. Benefits include improved functionality, improved performance, and improved power performance.

Result # 2 Relevance: ○○○○○

Method and Apparatus for the Placement of Signals Onto Lanes of a Byte Lane Selectable Bus to Provide Maximum Flexibility in Selecting Signal Groups

2001-06-10 IPCOM000014687D English (United States)

Method and Apparatus for the Placement of Signals Onto Lanes of a Byte Lane Selectable Bus to Provide Maximum Flexibility in Selecting Signal Groups The use of a programmable, byte lane selectable bus requires that the placement of the various processor units/signals be ...

Result # 3 Relevance: ○○○○○

Method for dynamic lockout avoidance in a SMT processor

2005-01-04 IPCOM000033913D English (United States)

In a simultaneous multi-threaded (SMT) processor, a thread may become "locked out" if it is blocked from making forward progress by the other thread(s). Disclosed is a method to dynamically avoid thread "lockout" by guaranteeing that each thread make ...

Result # 4 Relevance: ○○○○

Technique for Speculatively Sampling Performance Parameters

1994-09-01 IPCOM000113721D English (United States)

In multiprocessor systems using multiple caches whose coherency is managed by hardware, it is important to be able to provide information concerning the migration of cache lines from processor to processor. Measurements of existing multiprocessor systems show that cache ...

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Search query: (store queue or STQ) and (counter or timer)

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gathering store operations queue Search Advanced Search Preferences

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Gathering Store Instructions in a Superscalar Processor
the GPRs and the sequencer has determined that the **store operation** is non-speculative, then the **store** is put into the Committed **Store Queue** ...
www.priorartdatabase.com/IPCOM/000118096/ - Similar pages

POWER4 System Microarchitecture -- Page 4
The NCU Master includes a 4-deep FIFO **queue** for handling cache inhibited **stores**, including memory mapped I/O **store operations**, and cache and barrier ...
www-03.ibm.com/servers/eserver/ pseries/hardware/whitepapers/power4_4.html - 40k - Cached - Similar pages

Method and system for specualtively sending processor-issued **store** ...
The **gathering** of **stores** allows many different **store operations** targeting a given cache line to be absorbed by the **store queue** before the entry is sent to ...
www.freshpatents.com/ Method-and-system-for-specualtively-sending-processor-issued-**store-operations**-to-a-s... - 34k - Cached - Similar pages

National Partnership for Advanced Computational Infrastructure ...
30 Number of I = 1 **stores** (before **gathering**). 31 Number of **store** halfword ... 8 **Store queue** is full. 9 A master-generated **store operation** is stalled waiting ...
www.npaci.edu/Horizon/paraver/pmapi.html - 13k - Cached - Similar pages

GameTomorrow » XBOX 360 CPU Details Described at MPR Fall ...
Cacheable and Cache Inhibited **store operations** are processed through different pipelines. The cacheable **store** pipe includes 8 **store gathering** buffers per ...
gametomorrow.com/blog/index.php/2005/10/ 27/xbox-360-cpu-details-described-at-mpr-fall-processor-forum/ - 42k - Cached - Similar pages

Exchange 2000 Server **Operations** Guide: Enterprise Monitoring
Send **Queue** Size – This shows the **queue** of messages outbound from the Information **Store**. In situations where the SMTP service is down or there is a reduction ...
www.microsoft.com/technet/prodtechnol/ exchange/2000/maintain/e2kops4.mspx - 67k - Cached - Similar pages

[PDF] AN2424: MPC7410 and MPC7450, Comparison and Compatibility
File Format: PDF/Adobe Acrobat - View as HTML
Three basic types—execution, **store**, and. refetch. Issue **Queue** ... Performs **store gathering** only for. write-through **operations** to nonguarded ...
www.freescale.com/files/32bit/doc/app_note/AN2424.pdf - Similar pages

@(#)22 1.6 src/bos/usr/sbin/perf/pmapi/libpmapi/POWER3-II.evs ...
#35,u,n,PM_I_1_ST_TO_BUS,Number of I=1 **store operations** to bus Number of I=1 **store** ... #8,u,n,PM_STQ_FULL,**Store queue** is full **Store queue** is full. ...
www.cs.utk.edu/~terpstra/power4/POWER3-II.evs - 34k - Cached - Similar pages

Messaging Server Administrator's Guide: Monitoring and Maintaining ...
Both the **queue** and the **store** must have adequate disk space for the messages they ...
Each server **stores operation** information in the form of variables, ...
docs.sun.com/source/816-6044-10/maintain.htm - 98k - Cached - Similar pages

[PDF] SCI SOCKET - A Fast Socket Implementation over SCI
File Format: PDF/Adobe Acrobat - View as HTML
performed by a CPU posted **store operation** to the local I/O. system. **...** ceive **operations** every time the message **queue** status has **...**
www.gria.org/docs/sci-socket.pdf - Similar pages

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gathering store operations queue Search

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